ISSUE CLASSIFICATION	
Class	Subclass

PATENT NUMBER

U.S. UTILITY PATENT APPLICATION

O.I.P.E.	PATENT DATE
SCANNED Hkm 3 Q.A. 16	

APPLICATION NO.	CONT/PRIOR	CLASS	SUBCLASS	ART UNIT	EXAMINER
09/982413		~~365~~ 438	264	~~2818~~ 2823	

APPLICANTS: Sohrab Kianian
Chih Hsin Wang

TITLE: Self aligned method of forming a semiconductor memory array of floating gate memory cells with buried bitline and vertical word line transistor, and a memory array made thereby

PTO-2040
12/99

PREPARED AND APPROVED FOR ISSUE

ISSUING CLASSIFICATION

ORIGINAL		CROSS REFERENCE(S)	
CLASS	SUBCLASS	CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)

INTERNATIONAL CLASSIFICATION

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☐ Continued on Issue Slip Inside File Jacket

☐ TERMINAL DISCLAIMER	DRAWINGS			CLAIMS ALLOWED	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O.G.

☐ a) The term of this patent subsequent to _____ (date) has been disclaimed.

(Assistant Examiner) (Date)

NOTICE OF ALLOWANCE MAILED

☐ b) The term of this patent shall not extend beyond the expiration date of U.S Patent. No. _____

(Primary Examiner) (Date)

ISSUE FEE

Amount Due	Date Paid

☐ c) The terminal ____months of this patent have been disclaimed.

(Legal Instruments Examiner) (Date)

ISSUE BATCH NUMBER

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